Amendments to the Specification

Please replace the paragraph beginning on page 1, line 9 with the following amended paragraph:

A conventional high voltage MOS transistor has a structure wherein low-density diffused layers overlap with a gate electrode underneath the gate electrode to relax an electric field under the gate electrode to thereby suppress the occurrence of hot carriers. A method of manufacturing the conventional high voltage MOS transistor will be explained below with an N type MOS transistor as an example with reference to a process sectional ~~view of Fig. 3~~ views of Figs. 3(a) – 3(c).

Please replace the paragraph beginning on page 9, line 16 with the following amended paragraph:

Figs. 1(a) – 1(c) are ~~Fig. 1 is a~~ process sectional [[view]] views showing a method of manufacturing a semiconductor device according to a first embodiment, wherein Fig. 1(a) is a view subsequent to the formation of a gate electrode, Fig. 1(b) is a view subsequent to the implantation of an impurity, and ~~Fig 1(c)~~ Fig. 1(c) is a view subsequent to the formation of N type low-density diffused layers;

Please replace the paragraph beginning on page 9, line 23 with the following amended paragraph:

Figs. 2(a) and 2(b) show ~~Fig. 2 shows~~ a semiconductor device illustrating a

second embodiment, wherein Fig. 2(a) is a schematic sectional view of a device section, and Fig. 2(b) is a schematic plan view of the device section; and

Please replace the paragraph beginning on page 10, line 1 with the following amended paragraph:

Figs. 3(a) – 3(c) are ~~Fig. 3 is a~~ process sectional [[view]] views showing a conventional method of manufacturing a semiconductor device, wherein Fig. 3(a) is a view subsequent to the formation of N type low-density diffused layers, Fig. 3(b) is a view subsequent to the formation of a gate electrode, and Fig. 3(c) is a view subsequent to the formation of N type high-density diffused layers.

Please replace the paragraph beginning on page 10, line 18 with the following amended paragraph:

As a first embodiment, a method of manufacturing an N type MOS transistor will be explained here using [[a]] the process sectional views of Figs. 1(a) – 1(c) ~~view of Fig. 1~~, a sectional view of Fig. 2(a) and a schematic plan view of Fig. 2 (b) with the N type MOS transistor as an example. First, an insulating film 102 such as an oxide film used as a gate insulating film is formed about 100nm on a P type semiconductor layer 101 corresponding to a first conductivity type layer of a semiconductor substrate by using the known oxidation or CVD method.

Please replace the paragraph beginning on page 16, line 16 with the following amended paragraph:

The semiconductor device fabricated using the [[fist]] first embodiment will next be explained as a second embodiment. An N type MOS transistor will now be described as an example with reference to ~~Fig. 2~~ Figs. 2(a) – 2(b) in a manner similar to the first embodiment.